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EXAMINER	
QUILLEN, ALLEN E	

ART UNIT	PAPER NUMBER
2676	5

DATE MAILED: 11/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/837,043	Applicant(s) DOTSON, GARY DAN	
	Examiner Allen E. Quillen	Art Unit 2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Claims 1, 3, 5, 12, 17, 22 and 23 are amended for clarity. New claim 30 added. Claims 1-30 are pending. Applicant's arguments filed August 26, 2003 have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-11, 17-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuchkuda, et al, U.S. Patent 5,872,902 in view of Nishiyama, U.S. Patent 5,949,442.

5. Regarding claim 1, Kuchkuda discloses a video controller raster (Column 14, lines 34-41) engine (Figure 7, element 22, Column 10, lines 1-42) that receives video data from a frame

buffer and renders formatted data to a display in a computer system the raster engine comprising (Figure 8, Column 9, line 58 through Column 11, line 41): a first in first out (FIFO) memory (Figure 10B, element 44, Column 12, lines 15-35) that interfaces a host bus (Column 18, lines 6-9) in the computer system (Column 12, lines 42-46; Column 13, lines 6-7) with the raster engine and adapted to obtain video data from the frame buffer via the host bus and to provide video data to a video pipeline (Column 9, lines 61-64); a counter that has a value indicative of video data obtained from the frame buffer (Column 20 line 66 through Column 21, line 20; Column 18, lines 6-9); a counter that has a value indicative of video data, provided to the video pipeline (Column 18, lines 6-9); and a control logic system (Column 11, lines 1-2) associated with the FIFO memory, that provides an underflow (and overflow) indication (Figure 12A, Column 18, line 31 through Column 19, line 1).

Kuchkuda does not disclose that the counters are first input, first output and that the underflow indication is controlled according to the first input and output counter values. Nishiyama teaches a video controller (Figure 1, element 5, Column 1, lines 21, 54) using (a timer and) counters, a first input (Column 3, lines 7-10), a first output (CNT, Column 4, lines 24-29; Column 5, lines 28-29, 34, 40) and that the underflow indication is controlled (*prevent the occurrence of interruption*, Column 5, lines 52-53) according to the first input and output counter values (Column 3, lines 7-10, 29-30, 34-35; Column 5, lines 42-54). The motivation for combining a video controller, VRAM and FIFO design with underflow monitoring using counters is for display quality (*smooth scrolling*) and for efficiency (*lower hardware costs*) Column 1, lines 45-60). Nishiyama is evidence that at the time of the invention it would have been obvious to one skilled in the art of display design to incorporate the advantages of video

control features, as Kuchkuda discloses, with counters to prevent underflow, as Nishiyama teaches to achieve a smoother display with lower hardware costs.

6. Regarding claim 2, representative of claim 4, Kuchkuda and Nishiyama disclose a raster engine of claim 1, wherein the underflow indication comprises an underflow signal indicating at least one of an existing underflow condition, an anticipated underflow condition, and a raster engine lockup condition (see above, Kuchkuda, Column 18, lines 36-40; Column 21, lines 57-59; Column 27, lines 60-62; Column 25, lines 39-49; Figure 14, Column 26, lines 6-9, 19-26).

7. Regarding claim 3, Kuchkuda discloses a raster engine of claim 2, wherein the control logic system provides the underflow signal to a host (*workstation (WP),* Column 10, lines 3-4) processor in the computer system (Figures 7- 10, Column 11, lines 13-20).

8. Regarding claim 5, representative of claims 6, 8, 9, 17-24, 25-28 and 30, Kuchkuda discloses a raster engine of claim 4, wherein the raster engine comprises an underflow threshold value register programmable by a host processor in the computer system, and wherein the control logic system obtains the threshold value from the threshold value register (see above; Column 18, lines 6-10; Column 11, lines 1-2). Kuchkuda does not disclose compares the threshold value with the difference between the first input and output counter values. Nishiyama teaches compares the threshold value with the difference between the first input and output counter values (Figure 6, Column 5, lines 42-54; *15 equal the threshold value*).

The motivation for combining a video controller, VRAM and FIFO design with underflow monitoring using threshold values from counters is for display quality (*smooth scrolling*) and for efficiency (*lower hardware costs*) Column 1, lines 45-60). Nishiyama is evidence that at the time of the invention it would have been obvious to one skilled in the art of display design to incorporate the advantages of video control features, as Kuchkuda discloses, with counter values to prevent underflow, as Nishiyama teaches to achieve a smoother display with lower hardware costs.

9. Regarding claim 7, representative of claims 10, 11, 29, Kuchkuda discloses a raster engine of claim 6, wherein the FIFO memory obtains video data from the frame buffer according to a host (*40 MHz, RAMDAC,* Column 12, line 22; Column 19, lines 58-60) clock and provides video data to the video pipeline according to a video (*pixel,* Column 21, lines 3-4) clock, and wherein the underflow signal indicates an existing underflow condition when the counter values are equal for at least two cycles of the host clock (Column 19, line 1; Column 26, lines 19-25; Column 28, lines 58-60). Kuchkuda does not disclose first input and output counters; and an anticipated underflow condition when the first input and output counter values are within a threshold value of each other. Nishiyama teaches first input and output counters; and an anticipated underflow condition when the first input and output counter values are within a threshold value of each other (see above).

The motivation for combining a video controller, VRAM and FIFO design with underflow monitoring using threshold values from counters is for display quality (*smooth scrolling*) and for efficiency (*lower hardware costs*) Column 1, lines 45-60). Nishiyama is

evidence that at the time of the invention it would have been obvious to one skilled in the art of display design to incorporate the advantages of video control features, as Kuchkuda discloses, with counter values to prevent underflow, as Nishiyama teaches to achieve a smoother display with lower hardware costs.

Claim Rejections - 35 USC § 103

10. Claims 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuchkuda, et al, U.S. Patent 5,872,902 in view of Nishiyama, U.S. Patent 5,949,442 as applied to claim 1 above, and further in view of Rudin, et al, U.S. Patent 5,959,640 and Reddy, U.S. Patent 6,195,079.

11. Regarding claim 12, representative of claims 15-16, Kuchkuda and Nishiyama disclose a raster engine of claim 1, further comprising: an input counter value indicative of video data obtained from the frame buffer; and an output counter having output counter value indicative of video data provided to the video pipeline; wherein the raster engine selectively performs operation with the FIFO memory to provide video data to the video pipeline represented by the counter values; and wherein the control logic system provides an underflow indication according to the input and output counter values (see above). Kuchkuda and Nishiyama both disclose frame counters. Neither Kuchkuda nor Nishiyama disclose having a second input, second output, providing first and second video data to the video pipeline, nor do they disclose dual scan operation with the memory providing interleaved video.

Rudin discloses dual scan operation and interleaved video memory (Column 5, lines 14 – 30). The motivation for combining a video controller, VRAM and FIFO design, as Kuchkuda discloses, with underflow monitoring using threshold values from counters, as Nishiyama teaches, and further with dual scan and interleaved memory operations, as Rudin further teaches, is for display flexibility, particularly in LCD displays, and lower power consumption (Rudin, Column 1, lines 20-27, 48-50). Rudin is evidence that at the time of the invention, it would have been obvious for one skilled in the art of display controllers to combine the advantages of video controller, VRAM and FIFO design, disclosed by Kuchkuda, with underflow monitoring using threshold values from counters, as Nishiyama teaches, and further including LCD displays needing low power consumption available with dual display and interleaved memory operation, as Rudin teaches.

Reddy discloses a first and second input and outputs (*cathode ray tube, computer system memory or from an input device;* Column 1, lines 26-39; Column 2, lines 33-36; Figure 3, Column 6, lines 9-20, 59-66; Column 8, lines 48-50; Column 11, lines 56-60). The motivation for combining a video controller, VRAM and FIFO design with underflow monitoring using threshold values from counters, as Kuchkuda nor Nishiyama disclose, further with multiple inputs and outputs is to handle multiple display types (both LCD and CRT) and display requirements (Column 1, lines 52-66). Reddy is evidence that at the time of the invention it would have been obvious to one skilled in the art of display design to incorporate the advantages of video control features, as Kuchkuda and Nishiyama both disclose, that operate on multiple types of displays, as Reddy teaches, requiring first and second inputs and outputs due to the different display-type principles of operation.

12. Regarding claim 13, representative of claim 14, Kuchkuda and Nishiyama disclose a raster engine of claim 12, wherein the underflow indication comprises an underflow signal indicating at least one of an existing underflow condition, an anticipated underflow condition, and a raster engine lockup condition (see above, Kuchkuda, Column 18, lines 36-40; Column 21, lines 57-59; Column 27, lines 60-62; Column 25, lines 39-49; Figure 14, Column 26, lines 6-9, 19-26).

Response to Arguments

13. The Applicant argues that "Kuchkuda does not teach or suggest utilizing FIFO counter values, providing an underflow indication, or that an underflow indication is based on FIFO counter values..." (Page 9, bottom paragraph through Page 11, paragraph one).

14. The Examiner respectfully notes, however, that in the claims Kuchkuda and Nishiyama do disclose these features. Kuchkuda discloses control logic, line counters, page detection logic, underflow scheme to prevent starvation by managing memory in units of pages (Figure 12, Column 18, line 31 through Column 19, line 2). Nishiyama teaches that the underflow indication is controlled (*prevent occurrence of interruption*, Column 5, lines 52-53) according to the first input and output counter values (Column 3, lines 7-10, 29-30, 34-35; Column 5, lines 42-54).

15. The Applicant asserts that "Neither Rudin et al. nor Reddy overcome the deficiencies of Kuchkuda et al. and Nishiyama with respect to independent claim 1." (Page 11, last paragraph).

16. The Examiner respectfully replies that, in the claims 12-16 however, Rudin and Reddy teach the features of a second input, second output, providing first and second video data to the video pipeline, dual scan operation with the memory providing interleaved video for the purpose of low power consumption and multiple display types, as noted above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Allen E. Quillen whose telephone number is (703) 605-4584. The examiner can normally be reached on Tuesday – Friday, 8:30am – noon and 1:00 - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella, can be reached on (703) 308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or FAX'd to:

(703) 872-9314 (for Technology Center 2600 only)

Hand delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Sixth Floor (Receptionist), Arlington, Virginia

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number (703) 305-9600 or (703) 305-3800.

Allen E. Quillen
Patent Examiner
Art Unit 2676

***October 29, 2003

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600